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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,504	04/02/2004	Bernhard Knupfer	INFN/0076	3148

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PATTERSON & SHERIDAN, LLP
Gero McClellan / Infineon Technologies
3040 POST OAK BLVD.,
SUITE 1500
HOUSTON, TX 77056

EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/817,504	KNUPFER ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/2/004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-21 are in the application.

Claims 1-21 are rejected.

Drawing

Drawings of timing sequence of signals in Fig 2 and Fig 3 that describing the interrelationship among signals CM-I, CLK, DST, #A51, #A52, #A53, #A54, #A55 #A40 are requested.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3,10,12,17,19,21 rejected under 35 U.S.C. 103(a) as being unpatentable over Bando (US 2002/0145930).

As in claim 1, Bando describes a data memory circuit, comprising: a plurality of addressable memory cells (Bando's Fig 6: #22 memory array); a command-decoding device for decoding external commands (Bando's Fig 6: #12); a control device for controlling and initiating operations on the memory cells in response to the decoded commands (Bando's Fig 6: #20a); and a command buffer device for buffer-storing a command received in a critical operating state period during which execution of the command is impermissible and for releasing the command for execution after end of the critical operating state period (Bando's Fig 6: #14 buffering and storing external command; Bando's paragraphs 32-35 describes holding the external commands in #14 while executing the internal refresh command, and then executing the external command after the internal refreshing command is completed; see Fig 1).

As in claim 2, the claim recites wherein a plurality of critical operating states are possible, and in one or more critical operating states, a set of commands is impermissible; and wherein the command buffer device includes a buffer circuit assigned to each individual command of the set of impermissible commands (Bando's paragraph 30 describes circuit of Fig 2 capable of buffering external commands in various critical operation states, for example memory device's refresh states in refresh operations, while external read and write memory commands are not permitted).

As in claim 3, the claim recites wherein each buffer circuit comprises: a state evaluation circuit for generating a buffer standby signal during at least one operating state that is critical for the execution of respective impermissible command (Bando's paragraph 40 describes control

circuit Fig 2: #20 includes logic to hold information of the second command while executing the first command), and a logic circuit for setting a bi-stable element into a first state when the assigned command appears while the buffer standby signal is active and for re-generating the assigned command after the buffer standby signal has ended (Bando's paragraph 41 describes the read command is held back in the holding circuit and being re executed when the refresh operation is completed).

Claims 10,17 rejected based on the same rationale as in the rejection of claim 1.

Claims 12,19 rejected based on the same rationale as in the rejection of claim 3.

As in claim 21, the claim recites a method for controlling the execution of commands in a memory device comprising a plurality of addressable memory cells, the method comprising: receiving an external command while the memory device is performing a critical operation making execution of the external command impermissible; buffering the external command until the device completes the critical operation; and then executing the command. The claim rejected based on the same rationale as in the rejection of claim 1. Bando further describes the circuit to prevent the collision between the internal and external command (see Bando's paragraph 10).

Claims 4-9,11,13-16,18,20 rejected under 35 U.S.C. 103(a) as being unpatentable over Bando (US 2002/0145930).

As in claim 4, the claim recites wherein the command decoding device comprises: a predecoder, which, for each received command, activates a command line assigned to the received command (Bando's Fig 2: #12);

and an end decoder which excites selected enable lines of the control device depending on which of the command lines is activated. and wherein each buffer circuit is connected to a respectively assigned command line between the predecoder and the end decoder to receive the command from respective command line and to apply a re-generated command generated to respective command line.

Bando does not explicitly shows the output driver circuit (corresponding to the claim's end decoder) at the output of the latch that stores the command (corresponding to the claim's buffering circuit). However, Kirhata describes a refresh circuit as shown in Kirhata's Fig 6, that buffering and storing the external command (Kirhata's Fig 6: #624 latch transfers data to #623 latch; subsequently when xfer signal #685 is activated, data is transferred from #623 to ADDI address bus of a memory device, column 6 lines 37-66). It would have been obvious to one of ordinary skill in the art at the time of invention to include the buffering and forwarding circuits as suggested by Kirhata in Bando's system thereby external memory command such as activate can be held until the refresh operation is completed (Kirhata's column 5 lines 25-35).

As in claim 5, the claim recites wherein each buffer circuit includes a switch in a path of the respective command line, wherein the switch is opened precisely while a buffer standby signal is active to inhibit forwarding of an activation of the command line effected by the predecoder to the end decoder. The claim rejected based on the same rationale as in the rejection of claim 1. Kirhata's Fig 6 shows the xfer signal will not forward the information in latch #623 during the execution of refresh command.

As in claim 6, the claim recites wherein a source of external commands is adapted to a specification of the data memory circuit with regard to command-issuing times (Bando's control circuit determines when to issues the proper commands to the memory device),

and wherein the command buffer device handles external commands whose execution leads to termination of internally controlled processes in the data memory circuit (Kirhata's column 5 lines 35-50 describes a method wherein an activate command will leads to an execution and completion of an internal refresh operation in an automatic manner).

As in claim 7, the claim recites wherein the command buffer device handles external commands whose execution leads to termination of a self-controlled data-refresh process in the memory circuit. The claim rejected based on the same rationale as in the rejection of claim 6.

As in claim 8, the claim recites wherein the control device includes blockage elements for blocking execution of commands during the critical operating state period, and wherein the command buffer device directly forwards commands received during the critical operating state period. (Kirhata's Fig 6 shows the xfer signal will not forward the information in latch #623 during the execution of refresh command, however the refresh command is being forwarded to the memory device).

As in claim 9, the claim recites wherein the command buffer device inhibits forwarding of the received command to the control device during the critical operating state period (Kirhata's Fig 6 shows the xfer signal will not forward the information in latch #623 during the execution of refresh command).

Claims 11,18 rejected based on the same rationale as in the rejection of claim 4.

Claims 13,20 rejected based on the same rationale as in the rejection of claim 5.

Claim 14 rejected based on the same rationale as in the rejection of claim 8.

Claim 15 rejected based on the same rationale as in the rejection of claim 6.

Claim 16 rejected based on the same rationale as in the rejection of claim 7.

Conclusion

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan
5/24/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER

DD

Mano Padmanabhan

Supervisory Patent Examiner

TC2188